NEC

User's Manual

IE-784928-NS-EM1

Emulation Board

IE-784928-NS-EM1 EP-784928GF-NS

Target device μ PD784915 Subseries μ PD784928 Subseries μ PD784928Y Subseries

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INTRODUCTION

Product Overview

The IE-784928-NS-EM1 is designed to be used with the IE-78K4-NS and dedicated emulation probe to debug the following target devices that belong to the 78K/IV Series of 16-bit single-chip microcontrollers.

• μPD784915 Subseries: μPD784915, 784915A, 784915B, 784916A, 784916B,

78P4916

μPD784928 Subseries: μPD784927, 78F4928
 μPD784928Y Subseries: μPD784927Y, 78F4928Y

Target Readers

This manual is intended for engineers who will use the IE-784928-NS-EM1 with the IE-78K4-NS to perform system debugging.

Engineers who use this manual are expected to be thoroughly familiar with the target device's functions and use methods and to be knowledgeable about debugging.

Organization

When using the IE-784928-NS-EM1, refer to not only this manual (supplied with the IE-784928-NS-EM1) but also the manual that is supplied with the IE-78K4-NS.

IE-78K4-NS User's Manual

- Basic specifications
- System configuration
- External interface functions

IE-784928-NS-EM1 User's Manual

- General
- Part names
- Installation
- Differences between target devices and target interface circuits

Purpose

This manual's purpose is to explain various debugging functions that can be performed when using the IE-784928-NS-EM1.

Terminology

The meanings of certain terms used in this manual are listed below.

Term	Meaning
Emulation device	This is a general term that refers to the device in the emulator that is used to emulate the target device. It includes the emulation CPU.
Emulation CPU	This is the CPU block in the emulator that is used to execute user-generated programs.
Target device	This is the device (a real chip) that is the target for emulation.
Target system	The device that is targeted for debugging. This includes the target program and the hardware provided by the user. When defined narrowly, it includes only the hardware.
IE system	This refers to the combination of the IE-78K4-NS and the IE-784928-NS-EM1.

Conventions Data significance: Higher digits on the left and lower digits on the right

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

Remark: Supplementary information

Related Documents

The related documents (user's manuals) indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name	Document Number	
	English	Japanese
IE-78K4-NS	U13356E	U13356J
IE-784928-NS-EM1	This manual	U13819J
ID78K4-NS Integrated Debugger Reference Windows™ Based	U12796E	U12796J
μPD784915 Subseries Hardware	U10444E	U10444J
μPD784928 Subseries Hardware	U12648E	U12648J

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents when designing.

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CHAPTER 1 GENERAL

The IE-784928-NS-EM1 is a development tool for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K/IV Series of 16-bit single-chip microcontrollers.

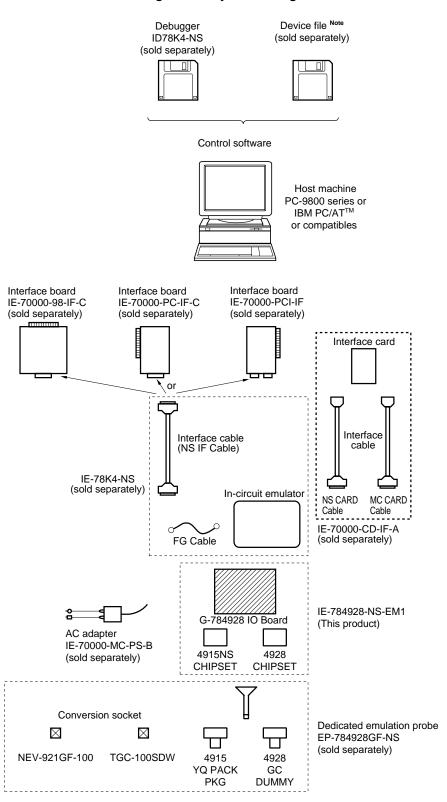
This chapter describes the IE-784928-NS-EM1's system configuration and basic specifications.

- Target device
 - μPD784915 Subseries
 - μPD784928 Subseries
 - μPD784928Y Subseries

1.1 System Configuration

Figure 1-1 illustrates the IE-784928-NS-EM1's system configuration.

Figure 1-1. System Configuration



CHAPTER 1 GENERAL

Note The device file is as follows, in accordance with the subseries.

 μ S×××DF784915: μ PD784915 Subseries

 μ S×××DF784928: μ PD784928, 784928Y Subseries

1.2 Hardware Configuration

Figure 1-2 shows the IE-784928-NS-EM1's position in the basic hardware configuration.

Dedicated bus interface IE system -----IE-78K4-NS----------IE-784928-NS-EM1 -----Interface board Host machine 78K4 main board I/O emulation board (sold separately) 4928 4915NS Interface card 78K4 emulation board chipset board chipset board (sold separately) Dedicated emulation probe EP-784928GF-NS (sold separately)

Figure 1-2. Basic Hardware Configuration

1.3 Basic Specifications

The IE-784928-NS-EM1's basic specifications are listed in Table 1-1.

Table 1-1. Basic Specifications

Parameter	Description
Target device	μPD784915, 784928, 784928Y Subseries
System clock	Main system clock: 8 MHz Subsystem clock: 32.768 kHz
Main clock supply	External: Input via an emulation probe from the target system Internal: Mounted on emulation board (16 MHz), or mounted on the board by the user
Subsystem clock supply	Internal: Mounted on emulation board (32.768 kHz)
Low-voltage support	2.7 V or higher (same as target device)

[MEMO]

CHAPTER 2 PART NAMES

This chapter introduces the parts of the IE-784928-NS-EM1 main unit and the chipset boards.

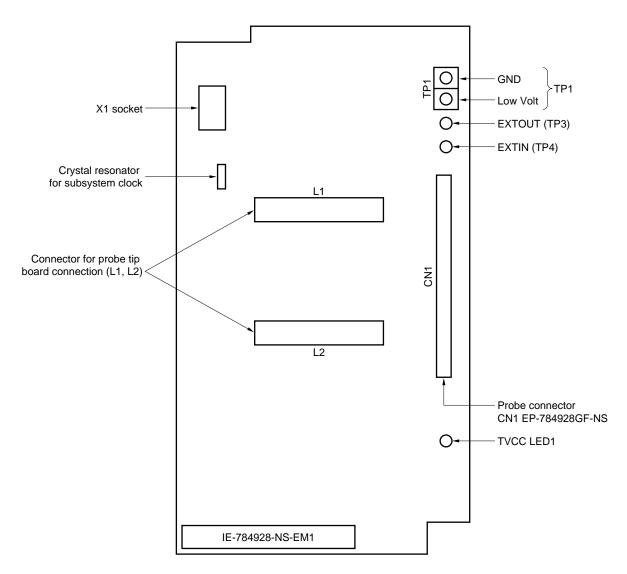
The packing box contains the emulation board (IE-784928-NS-EM1), and two chipset boards (4915NS CHIPSET, 4928 CHIPSET).

If there are any missing or damaged items, please contact an NEC sales representative.

Fill out and return the guarantee document that comes with the main unit.

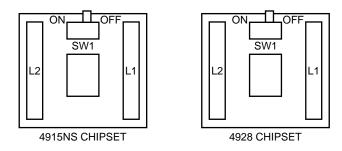
2.1 Parts of Emulation Board

Figure 2-1. IE-784928-NS-EM1 Part Names



2.2 Chipset Board Part Names

Figure 2-2. Chipset Board Part Names



The IE-784928-NS-EM1 includes the 4915NS CHIPSET and the 4928 CHIPSET.

- (1) When the 4915NS CHIPSET is used to emulate the μ PD784915 Subseries, use the 4928 CHIPSET to emulate the μ PD784928 and 784928Y Subseries.
- (2) When using an emulation probe, connect the 4915NS CHIPSET or the 4928 CHIPSET to the probe tip.
- (3) When not using an emulation probe, connect the 4915NS CHIPSET or the 4928 CHIPSET to the L1 and L2 connectors on the IE-784928-NS-EM1.

Caution Do not connect the chipset boards to both the emulation probe tip and the L1 and L2 connectors on the IE-784928-NS-EM1 at the same time.

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CHAPTER 3 INSTALLATION

This chapter describes methods for connecting the IE-784928-NS-EM1 to the IE-78K4-NS, emulation probe, or chipset boards. Mode setting methods are also described.

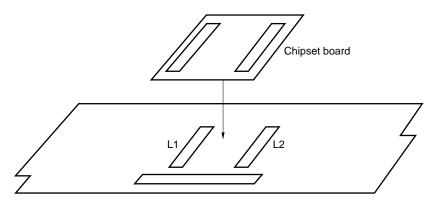
Caution Connecting or removing components to or from the target system, or making switch or other setting changes must be carried out after the power supply to both the IE system and the target system has been switched OFF.

3.1 Connection

(1) Connection to chipset board

Connect the 4915NS CHIPSET or the 4928 CHIPSET to the L1 and L2 connectors on the IE-784928-NS-EM1.

Figure 3-1. Mounting of Chipset Board



Caution Do not connect the chipset board while the emulation probe is in use.

(2) Connection with IE-78K4-NS main unit

See the IE-78K4-NS User's Manual (U13356E) for a description of how to connect the IE-784928-NS-EM1 to the IE-78K4-NS.

(3) Connection with emulation probe

See CHAPTER 4 EMULATION PROBE (EP-784928GF-NS) for a description of how to connect an emulation probe to the IE-784928-NS-EM1.

On this board, connect the emulation probe to CN1.

Caution A clock cannot be supplied to the emulation device from the oscillation clock in the target system. When operating at a frequency other than 16 MHz, attach a clock device of the same oscillation frequency as that supplied to the target device to X1.

3.2 Target Device Setting

When emulating the μ PD784915 Subseries, connect the 4915NS CHIPSET to L1 and L2. When emulating the μ PD784928 and μ PD784928Y Subseries, connect the 4928 CHIPSET to L1 and L2.

3.3 Clock Settings

3.3.1 Overview of clock settings

The main system clock to be used during debugging can be selected from (1) to (3) below.

- (1) Clock that is already mounted on emulation board
- (2) Clock that is mounted by user
- (3) External clock

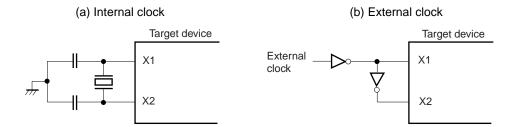
Caution Use "clock that is already mounted on emulation board" for the subsystem clock.

If the target system includes an internal clock, select either "(1) Clock that is already mounted on emulation board" or "(2) Clock that is mounted by user". For an internal clock, the target device is connected to a resonator and the target device's internal oscillator is used. An example of the external circuit is shown in part (a) of Figure 3-2. During emulation, the resonator that is mounted on the target system is not used. Instead, the clock that is mounted on the emulation board, which is installed for the IE-78K4-NS is used.

If the target system includes an external clock, select "(3) External clock".

For an external clock, a clock signal is supplied from outside of the target device and the target device's internal oscillator is not used. An example of the external circuit is shown in part (b) of Figure 3-2.

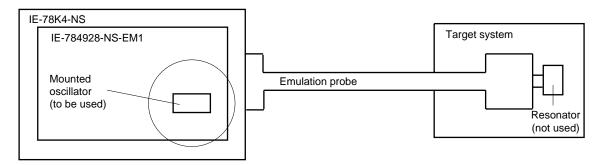
Figure 3-2. External Circuits Used as System Clock Oscillator



(1) Clock that is already mounted on emulation board

A crystal oscillator is already mounted on the emulation board. Its frequency is 16 MHz.

Figure 3-3. When Using Clock That Is Already Mounted on Emulation Board



Remark The clock that is supplied by the IE-784928-NS-EM1's oscillator (encircled in the figure) is used.

(2) Clock that is mounted by user

The user is able to mount any clock supported by the set specifications on the IE-784928-NS-EM1. First mount the resonator on the parts board, then attach the parts board to the IE-784928-NS-EM1. This method is useful when using a different frequency from that of the pre-mounted clock.

IE-78K4-NS
IE-784928-NS-EM1

Parts board

Resonator (to be used)

Resonator (not used)

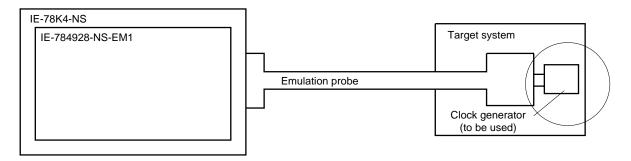
Figure 3-4. When Using User-Mounted Clock

Remark The clock that is supplied by the IE-784928-NS-EM1's resonator (encircled in the figure) is used.

(3) External clock

An external clock connected to the target system can be used via an emulation probe.

Figure 3-5. When Using an External Clock



Remark The clock supplied by the target system's clock generator (encircled in the figure) is used.

3.3.2 Main system clock settings

Table 3-1. Main System Clock Settings

Frequency of Main System Clock		IE-784928-NS-EM1	CPU Clock Source
		Parts Board (X1)	Selection (ID)
When using clock that is already mounted on emulation board	16 MHz	Oscillator used	Internal
When using clock mounted by user	Other than 16 MHz	Oscillator assembled by user	
When using external clock		Oscillator not used	External

Caution When using an external clock, open the configuration dialog box when starting the integrated debugger (ID78K4-NS) and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user's clock).

Remark The IE-784928-NS-EM1's factory settings are those listed above under "when using clock that is already mounted on emulation board".

(1) When using clock that is already mounted on emulation board

When the IE-784928-NS-EM1 is shipped, a 16-MHz crystal oscillator is already mounted in the IE-784928-NS-EM1's X1 socket. When using the factory-set mode settings, there is no need to make any other hardware settings.

When starting the integrated debugger (ID78K4-NS), open the configuration dialog box and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).

(2) When using clock mounted by user

The settings described under either (a) or (b) are required, depending on the type of clock to be used. When starting the integrated debugger (ID78K4-NS), open the configuration dialog box and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).

(a) When using a ceramic resonator or crystal resonator

- Items to be prepared
 - Parts board (supplied with IE-78K4-NS)
 - Ceramic resonator or crystal resonator
 - Resistor Rx

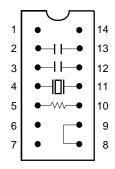
- Capacitor CA
- Capacitor CB
- Solder kit

<Steps>

<1> Solder the target ceramic resonator or crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequency) onto the supplied parts board (as shown below).

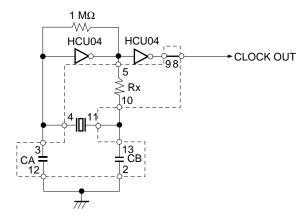
Figure 3-6. Connections on Parts Board (When Using Main System Clock or User-Mounted Clock)

Parts board (X1)



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic resonator or crystal resonator
5-10	Resistor Rx
8-9	Short

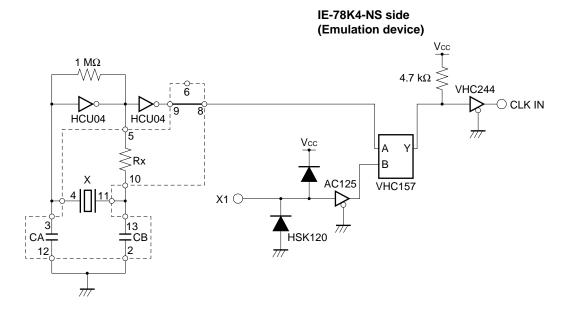
Circuit diagram



Remark The sections enclosed in broken lines indicate parts that are attached to the parts board.

- <2> Prepare the IE-784928-NS-EM1.
- <3> Remove the crystal oscillator that is mounted in the IE-784928-NS-EM1's socket (the socket marked as X1).
- <4> Connect the parts board (from <1> above) to the socket (X1) from which the crystal oscillator was removed. Check the pin 1 mark to make sure the board is mounted in the correct direction.
- <5> Make sure that the parts board mounted in the X1 socket on the emulation board is wired as shown in Figure 3-6 above.
- <6> Install the IE-784928-NS-EM1 in the IE-78K4-NS.

The above steps configure the following circuit and enable supply of the clock from the mounted resonator to the emulation device.

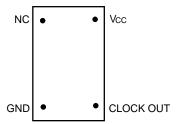


Remark The sections enclosed in broken lines indicate parts that are attached to the parts board.

(b) When using a crystal oscillator

- Items to be prepared
 - Crystal oscillator (see pinouts shown in Figure 3-7)

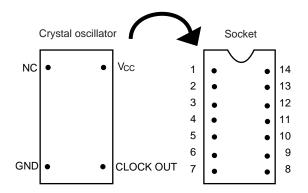
Figure 3-7. Crystal Oscillator (When Using Main System Clock or User-Mounted Clock)



<Steps>

- <1> Prepare the IE-784928-NS-EM1.
- <2> Remove the crystal oscillator that is mounted in the IE-784928-NS-EM1's socket (the socket marked as X1).
- <3> Connect the crystal oscillator (from <2> above) to the socket (X1) from which the crystal oscillator was removed. Insert the crystal oscillator pin into the socket aligning the pins as shown in the figure below.

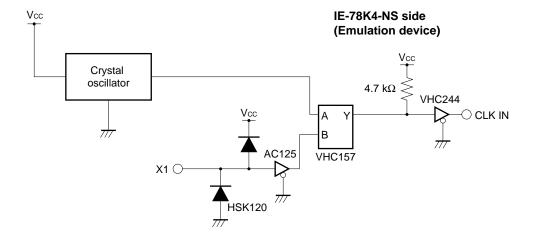
Figure 3-8. Pin Alignment of Crystal Oscillator and Socket



Crystal Oscillator Pin Name	Socket Pin No.
NC	1
GND	7
CLOCK OUT	8
Vcc	14

<4> Install the IE-784928-NS-EM1 in the IE-78K4-NS.

The above steps configure the following circuit and enable supply of the clock from the mounted resonator to the emulation device.



(3) When using external clock

No hardware settings are required for this situation.

When starting the integrated debugger (ID78K4-NS), open the configuration dialog box and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user's clock).

3.3.3 Subsystem clock settings

When the IE-784928-NS-EM1 is shipped, a 32.768-kHz crystal resonator is already mounted in the IE-784928-NS-EM1.

The system clock cannot be changed.

3.4 Pin Mask Function Settings

• NMI interrupt mask setting

By setting a switch (SW1) on the 4915NS CHIPSET, or 4928 CHIPSET in the IE-784928-NS-EM1, it is possible to mask the NMI interrupt, which is the alternate function of the P20 pin.

Table 3-2. Slide Switch Setting for NMI Interrupt Mask Function

Status	Slide Switch Setting
	SW1
No NMI mask (initial setting)	OFF
NMI masked	ON

Caution Because the NMI interrupt is the alternate function of the P02/INTP2 pin, this pin cannot operate as the P02/INTP2 pin when the NMI mask status has been set.

3.5 Low-Voltage Emulation Setting

Low-voltage emulation is possible in the IE system.

When the target system is operating on low voltage, supply the same voltage as the target system to the TP1 terminal pin of the IE-784928-NS-EM1 (this is unnecessary when TP1 is 5 V). Set the target voltage between 2.7 and 5 V.

• Maximum current consumption of TP1

5 V 300 mA

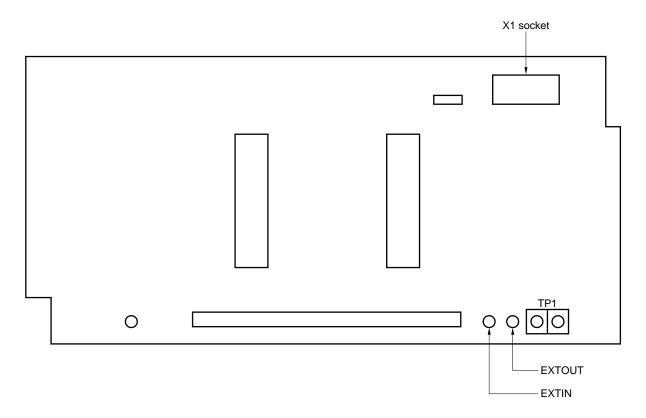
2.7 V 150 mA

3.6 External Trigger

To set up an external trigger, connect it to the IE-784928-NS-EM1's check pin, EXTOUT pin, and EXTIN pin as shown below.

See the integrated debugger (ID-78K4-NS) User's Manual (U12796E) for descriptions of related use methods and pin characteristics.

Figure 3-9. External Trigger Input Position



[MEMO]

CHAPTER 4 EMULATION PROBE (EP-784928GF-NS)

When using the IE-784928-NS-EM1 connected to the target system, a dedicated emulation probe (EP-784928GF-NS: sold separately) is needed.

Using the EP-784928GF-NS for connection enables debugging of the hardware and software of the target system in which the μ PD784915, μ PD784928, or μ PD784928Y Subseries are employed. For connection details, refer to **4.2 Connection Procedure**.

4.1 Configuration of EP-784928GF-NS

The configuration of the EP-784928GF-NS is described below.

- EP-784928GF-NS
- Probe tip board (DUMMY BOARD): 4915 YQ PACK PKG (100GF)
- Probe tip board (DUMMY BOARD): 4928 GC DUMMY (100GC)
- Conversion socket: NEV921GF-100
- Conversion socket: TGC-100SDW

Caution Chipset boards are not included with the EP-784928GF-NS, so use the 4915 NS CHIPSET and 4928 CHIPSET included with the IE-784928-NS-EM1.

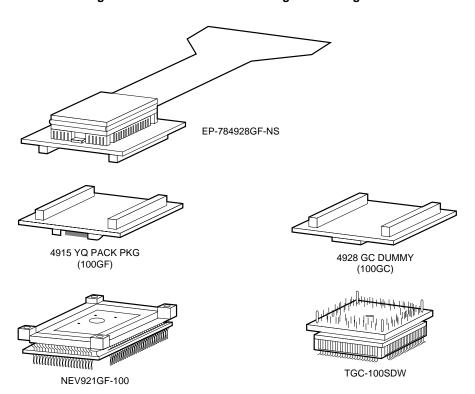


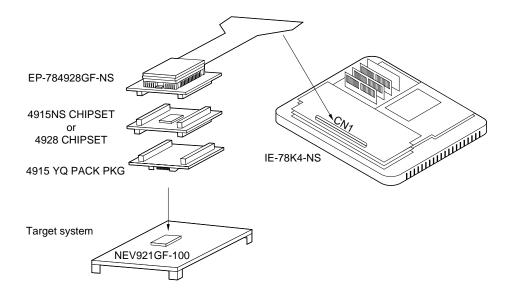
Figure 4-1. EP-784928GF-NS Configuration Diagram

4.2 Connection Procedure

4.2.1 Emulation probe and target system connection (when using the 100-pin GF package)

- (1) Solder the accompanying conversion socket (NEV921GF-100) to the target system.
- (2) Connect the 4915 YQ PACK PKG (DUMMY BOARD) to the soldered conversion socket (NEV921GF-100), and fix with screws.
- (3) Plug the emulation probe tip into the 4915 YQ PACK PKG (DUMMY BOARD).

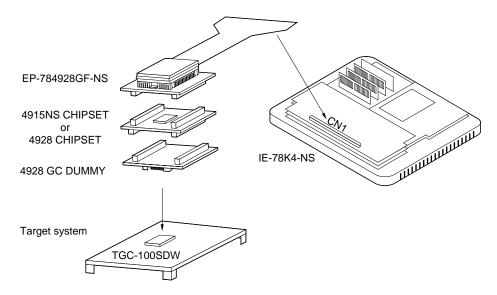
Figure 4-2. Emulation Probe and Target System Connection (When Using the 100-Pin GF Package)



4.2.2 Emulation probe and target system connection (when using the 100-pin GC package)

- (1) Solder the accompanying conversion socket (TGC-100SDW) to the target system.
- (2) Connect the 4928 GC DUMMY (DUMMY BOARD) to the soldered conversion socket (TGC-100SDW), and fix with screws.
- (3) Plug the emulation probe tip into the 4928 GC DUMMY (DUMMY BOARD).

Figure 4-3. EP-784928GF-NS and Target System Connection (When Using the 100-Pin GC Package)



[MEMO]

CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS

This chapter describes differences between the target device's signal lines and the signal lines of the IE-784928-NS-EM1's target interface circuit.

Although the target device is a CMOS circuit, the IE-784928-NS-EM1's target interface circuit consists of an emulation CPU, TTL, CMOS-IC, and other emulation circuits.

When the IE system is connected with the target system for debugging, the IE system performs emulation so as to operate as the actual target device would operate in the target system.

However, some minor differences exist since the operations are performed via the IE system's emulation.

- (1) Signals directly input/output to/from the emulation CPU
- (2) Signals input from the target system via a gate
- (3) Other signals

The IE system's circuit is used as follows for signals listed in (1) to (3) above.

(1) Signals directly input/output to/from the emulation CPU

The following signals perform the same operations as in the μ PD784915, 784928 Subseries. For the signals related to ports 0, 4, and 5, a 22- Ω resistor is inserted in series. The NMI performs mask control by means of SW1 on the chipset board.

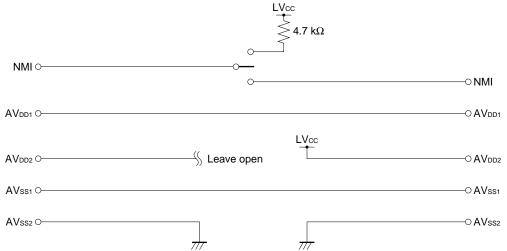
- Signals related to port 0
- · Signals related to port 4
- Signals related to port 5
- Signals related to port 6
- Signals related to port 7 (A/D converter input)
- Signals related to port 8
- Signals related to port 9
- Signals related to external input (INTP0 to INTP2)
- Signals related to timer output (PT00 to PT02)
- Signals related to serial communication (SCK2, SO2, SI2/BUSY)
- Signals related to A/D converter (ANI08 to ANI11)
- NMI

Figure 5-1. Equivalent Circuit 1 of Emulation Circuit

P00 to P07 ○ 22 Ω P40 to P47 ○ 1 MΩ P50 to P57 ○ 1 MΩ P50 to P57 ○ 1 MΩ P50 to P57 ○ P50 to P57 P60 to P67 ○ ○ P60 to P67 P70 to P77 ○ ○ P70 to P77 P80 to P87 ○ ○ P80 to P87 P90 to P96 ○ ○ P90 to P96 REEL0IN ○ ○ REEL0IN REEL1IN ○ ○ REEL1IN CSYNCIN ○ ○ CSYNCIN DFGIN ○ ○ DFGIN CFGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ ○ RECCTL+ CTLIN ○ ○ CTLIN	Probe side		IE system side
P40 to P47 ○ ○ P40 to P47 P50 to P57 ○ ○ P50 to P57 P60 to P67 ○ ○ P60 to P67 P70 to P77 ○ ○ P70 to P77 P80 to P87 ○ ○ P80 to P87 P90 to P96 ○ ○ P90 to P96 REELOIN ○ ○ REELOIN REELIIN ○ ○ REELIIN CSYNCIN ○ ○ CSYNCIN DFGIN ○ ○ DFGIN CFGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ RECCTL+ CTLIN ○ ○ CTLIN	P00 to P07 O	───	○ P00 to P07
P60 to P67 ○ ○ P60 to P67 P70 to P77 ○ ○ P70 to P77 P80 to P87 ○ ○ P80 to P87 P90 to P96 ○ ○ P90 to P96 REELOIN ○ ○ REELOIN REEL1IN ○ ○ REEL1IN CSYNCIN ○ ○ CSYNCIN DFGIN ○ ○ DFGIN CFGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ RECCTL+ CTLIN ○ ○ CTLIN	P40 to P47 O		───○ P40 to P47
P60 to P67 ○ ○ P60 to P67 P70 to P77 ○ ○ P70 to P77 P80 to P87 ○ ○ P80 to P87 P90 to P96 ○ ○ P90 to P96 REELOIN ○ ○ REELOIN REEL1IN ○ ○ REEL1IN CSYNCIN ○ ○ CSYNCIN DFGIN ○ ○ DFGIN CFGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ RECCTL+ CTLIN ○ ○ CTLIN	P50 to P57 O	22 Ω ////	P50 to P57
P80 to P87 ○ ○ P80 to P87 P90 to P96 ○ ○ P90 to P96 REELOIN ○ ○ REELOIN REELIIN ○ ○ REELIIN CSYNCIN ○ ○ CSYNCIN DFGIN ○ ○ DFGIN DPGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ RECCTL+ CTLIN ○ ○ CTLIN	P60 to P67 O	////	○ P60 to P67
P90 to P96 ○ ○ P90 to P96 REEL0IN ○ ○ REEL0IN REEL1IN ○ ○ CSYNCIN DFGIN ○ ○ DFGIN DPGIN ○ ○ DPGIN CFGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CTLDLY RECCTL+ ○ ○ RECCTL+ CTLIN ○ ○ CTLIN	P70 to P77 O		──── P70 to P77
REELOIN ○ ○ REELOIN REEL1IN ○ ○ REEL1IN CSYNCIN ○ ○ CSYNCIN DFGIN ○ ○ DFGIN DPGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ ○ RECCTL+ CTLIN ○ ○ CTLIN	P80 to P87 O		
REEL1IN ○ ○ REEL1IN CSYNCIN ○ ○ CSYNCIN DFGIN ○ ○ DFGIN DPGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ RECCTL+ CTLIN ○ ○ CTLIN	P90 to P96 O		○ P90 to P96
CSYNCIN ○ ○ CSYNCIN DFGIN ○ ○ DFGIN DPGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ RECCTL+ CTLIN ○ ○ CTLIN	REEL0IN O-		
DFGIN ○ ○ DFGIN DPGIN ○ ○ DPGIN CFGIN ○ ○ CFGIN CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ RECCTL+ RECCTL- ○ CTLIN	REEL1IN O-		○REEL1IN
DPGIN ○ ○ DPGIN CFGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CTLDLY ○ ○ CTLDLY RECCTL+ ○ ○ RECCTL+ CTLIN ○ ○ CTLIN	CSYNCIN O-		
CFGIN ○ ○ CFGIN CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ ○ RECCTL+ CTLIN ○ ○ CTLIN	DFGIN ○		○ DFGIN
CFGAMPO ○ ○ CFGAMPO CFGCPIN ○ ○ CFGCPIN CTLDLY ○ ○ CTLDLY RECCTL+ ○ ○ RECCTL+ RECCTL- ○ ○ CTLIN	DPGIN ○		○ DPGIN
CFGCPIN	CFGIN ○		
CTLDLY 0 OCTLDLY RECCTL+0 ORECCTL+ RECCTL-0 ORECCTL- CTLIN 0 OCTLIN	CFGAMPO O		○ CFGAMPO
RECCTL+○ ○RECCTL+ RECCTL-○ ○RECCTL- CTLIN○ ○CTLIN	CFGCPIN ○		
RECCTL— ORECCTL— CTLIN O CTLIN	CTLDLY O		○ CTLDLY
CTLIN O	RECCTL+ O		
CTLIN O	RECCTL-O		○RECCTL -
CTLOUT2 O			

Figure 5-2. Equivalent Circuit 2 of Emulation Circuit



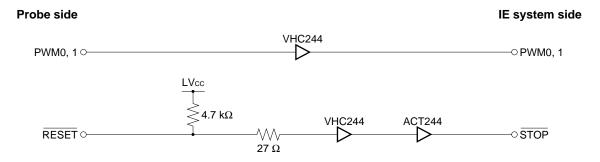


(2) Signals input from the target system via a gate

Since the following signals are input via a gate, their timing shows a delay compared to that of the μ PD784915, 784928 Subseries. Their AC characteristics and DC characteristics are therefore different from the μ PD784928 Subseries, making it necessary to observe a stricter timing design than in the case of the μ PD784915, 784928 Subseries.

- PWM0, PWM1
- RESET signal

Figure 5-3. Equivalent Circuit 3 of Emulation Circuit



(3) Other signals

• VDD pin

When the emulation CPU is operating at 5 V, its power is supplied from the internal IE system, but when operating at low voltage, its power is supplied from the low-voltage pin (TP1). The V_{DD} pin of the target system is only used to control the LED (USERV_{DD}) in the IE system that monitors the input of the target system's power supply.

• Vss pin

The Vss pin is connected to GND inside the IE system.

[MEMO]

[MEMO]



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